ACPL-336J

2.5 Amp Gate Drive Optocoupler with Integrated (V_{CE}) Desaturation Detection, Active Miller Clamping, Fault and UVLO Status Feedback

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

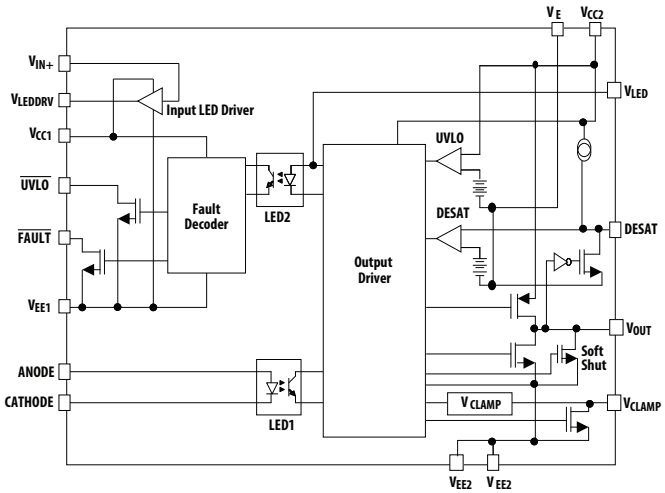
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

Avago's ACPL-336J gate drive optocoupler features fast propagation delay with excellent timing skew performance. Smart features that are integrated to protect the IGBT include IGBT desaturation detection with soft-shutdown protection and fault feedback, undervoltage lockout and feedback, and active Miller current clamping. This full-featured and easy-to-implement IGBT gate drive optocoupler comes in a compact, surface-mountable SO-16 package for space-savings. It is suitable for driving IGBTs and power MOSFETs used in motor control and inverter applications.

Avago isolation products provide reinforced insulation and reliability that deliver safe signal isolation critical in high voltage and noisy industrial applications.

Functional Diagram



Features

- 2.5 A maximum peak output current
- Rail-to-rail output voltage
- 2.0 A Miller clamp sinking current
- Integrated fail-safe IGBT protection
  - Desaturation detection, "Soft" IGBT turn-off and fault feedback
  - UnderVoltage LockOut (UVLO) Protection with feedback
- Integrated input LED driver
- 250 ns maximum propagation delay over temperature
- 30 kV/μs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- Wide operating voltage: 15 V to 30 V
- Wide operating temperature range: -40 °C to 105 °C
- SO-16 package with 8 mm clearance and creepage
- Regulatory approvals:
  - UL 1577, V_{ISO} = 5000 V_{RMS} for 1 min
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1414 V_{PEAK}

Applications

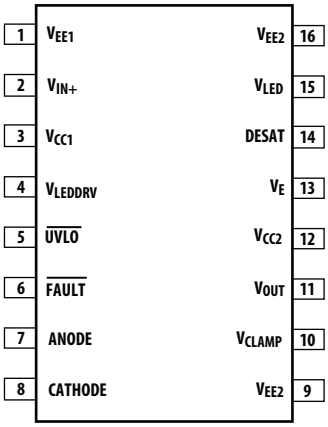
- Isolated IGBT/Power MOSFET gate drive
- Renewable energy inverters
- AC and brushless DC motor drives
- Industrial Inverters
- Switching power supplies

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Product Overview Description

The ACPL-336J is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit. It features IGBT desaturation detection with soft-shutdown protection and fault feedback, undervoltage lockout and feedback, and active Miller current clamping in a SO-16 package. Direct LED input with or without integrated LED driver allows flexible logic configuration and differential current mode driving with low input impedance, greatly increasing its noise immunity.

Pin Description



Pin	Symbol	Description
1	V_{EE1}	Input common
2	V_{IN+}	Non inverting voltage control input.
3	V_{CC1}	Input power supply (4.5 V to 5.5 V)
4	V_{LEDDRV}	Integrated LED driver output.
5	$\overline{UVLO}$	V_{CC2} undervoltage lockout feedback
6	$\overline{FAULT}$	DESAT fault feedback
7	ANODE	Input LED anode
8	CATHODE	Input LED cathode
9	V_{EE2}	Negative power supply
10	V_{CLAMP}	Miller current clamping output
11	V_{OUT}	Driver output to IGBT gate
12	V_{CC2}	Positive power supply
13	V_E	Common (IGBT emitter) output supply voltage.
14	DESAT	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 7 V while the IGBT is on, V_{OUT} will soft shut down and FAULT will change from High impedance to Low logic state
15	V_{LED}	No connection, for testing only
16	V_{EE2}	Negative power supply

Ordering Information

ACPL-336J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

	Option					
Part number	RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-336J	-000E	SO-16	X		X	45 per tube
	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

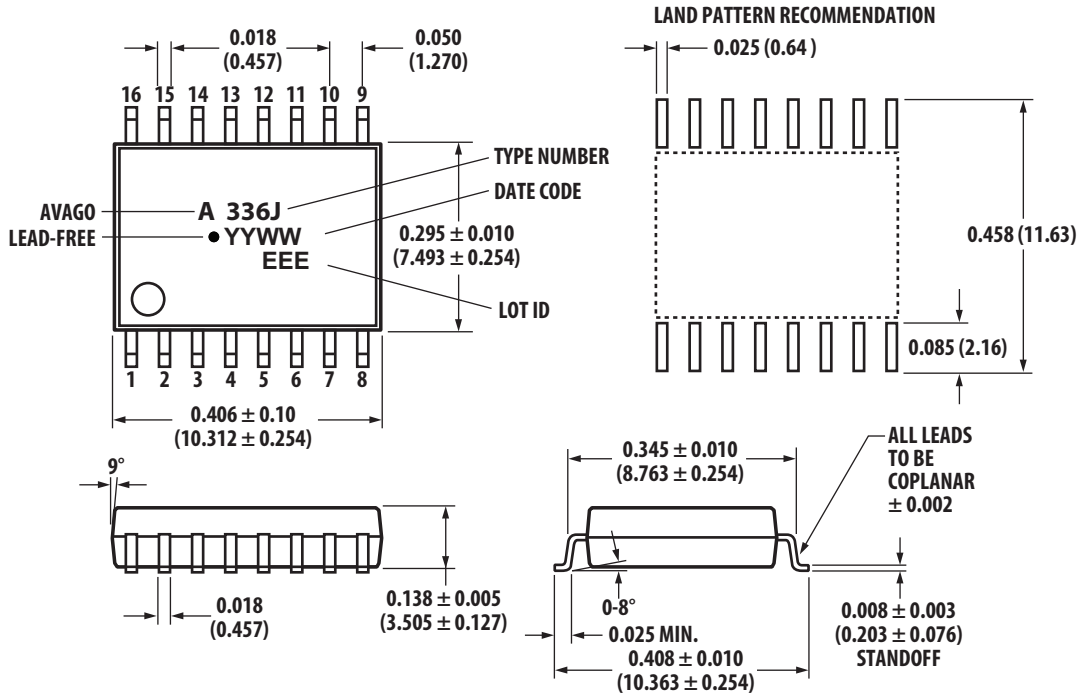
Example 1:

ACPL-336J-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-336J 16-Lead Surface Mount Package



Dimensions in inches (millimeters)

Notes: Initial and continued variation in the color of the ACPL-336J's white mold compound is normal and does note affect device performance or reliability.

Lead coplanarity = 0.1 mm (0.004 inches)

Floating Lead Protrusion is 0.25 mm (10 mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-336J is approved by the following organizations:

IEC/EN/DIN EN 60747-5-5

Maximum working insulation voltage V_{IORM} = 1414 V_{PEAK}

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/39, Table 1			
for rated mains voltage ≤ 150 V_{RMS}		I – IV	
for rated mains voltage ≤ 300 V_{RMS}		I – IV	
for rated mains voltage ≤ 600 V_{RMS}		I – IV	
for rated mains voltage ≤ 1000 V_{RMS}		I – III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b** V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a** V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	400	mA
Output Power	$P_{S, OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

** Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-336J	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J		125	°C	
Average Input Current	$I_{F(AVG)}$		20	mA	1
Peak Transient Input Current (< 1 μs pulse width, 300 pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		5	V	
Peak Output Current	$\|I_{O(PEAK)}\|$		2.5	A	2
$\overline{\text{FAULT}}$ Output Current	$I_{\overline{FAULT}}$		10	mA	
$\overline{\text{FAULT}}$ Pin Voltage	$V_{\overline{FAULT}}$	-0.5	V_{CC1}	V	
$\overline{\text{UVLO}}$ Output Current	$I_{\overline{UVLO}}$		10	mA	
$\overline{\text{UVLO}}$ Pin Voltage	$V_{\overline{UVLO}}$	-0.5	V_{CC1}	V	
Non Inverting Voltage Control Input Voltage	V_{IN+}	-0.5	V_{CC1}	V	
Integrated LED Driver Output Current	I_{LEDDRV}		20	mA	
Integrated LED Driver Output Voltage	V_{LEDDRV}	-0.5	V_{CC1}	V	
Positive Input Supply Voltage	V_{CC1}	-0.5	7.0	V	
Total Output Supply Voltage	$V_{CC2} – V_{EE2}$	-0.5	35	V	
Negative Output Supply Voltage	$V_E – V_{EE2}$	-0.5	15	V	3
Positive Output Supply Voltage	$V_{CC2} – V_E$	-0.5	$35 – (V_E – V_{EE})$	V	
Gate Drive Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC2}	V	
Peak Clamping Sinking Current	I_{CLAMP}		2	A	2
Miller Clamping Pin Voltage	V_{CLAMP}	-0.5	V_{CC2}	V	
DESAT Voltage	V_{DESAT}	$V_E – 0.5$	$(V_{CC2} + 0.5)$	V	
Output IC Power Dissipation	P_O		600	mW	4
Input LED Power Dissipation	P_I		150	mW	5

Notes:
1. Derate linearly above 70 °C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 μs
3. This supply is optional and is required only when negative gate drive is implemented.
4. Derate linearly above 95 °C free-air temperature at a rate of 20 mW/°C.
5. Derate linearly above 95 °C free-air temperature at a rate of 5 mW/°C. The maximum LED junction temperature should not exceed 125 °C.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	-40	105	°C	
Input supply voltage	V_{CC1}	4.5	5.5	V	1
Total Output Supply Voltage	$V_{CC2} – V_{EE2}$	15	30	V	2
Negative Output Supply Voltage	$(V_E – V_{EE})$	0	13.5	V	3
Positive Output Supply Voltage	$V_{CC2} – V_E$	15	$30 – (V_E – V_{EE})$	V	
Input LED Current	$I_{F(ON)}$	9	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V	

Notes:
1. In most applications V_{CC1} will be powered up first (before V_{CC2}) and powered down last (after V_{CC2}). This is desirable for maintaining control of the IGBT gate. In applications where V_{CC2} is powered up first, it is important to ensure that input remains low until V_{CC1} reaches the proper operating voltage (minimum 4.5 V) to avoid any momentary instability at the output during V_{CC1} ramp-up or ramp-down.
2. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 13.7 V.
3. This supply is optional and is required only when negative gate drive is implemented.

Table 5. Electrical Specifications (DC)

Unless otherwise noted, all typical values at T_A = 25 °C, V_{CC1} = 5 V, V_{CC2} – V_{EE2} = 30 V, V_E – V_{EE2} = 0 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Logic Low Input Voltage	V_{IN+L}			0.8	V		23	
Logic High Input Voltage	V_{IN+H}	2			V		23	
Logic High LED Driver Output $R_{DS(ON)}$	$R_{LEDDRVH}$	5.5	13.5	24	Ω	I_{LEDDRV} = -10 mA, V_{IN+} = 5 V	23	
Logic Low LED Driver Output Voltage	$V_{LEDDRVL}$	0.2	0.4	0.8	V	I_{LEDDRV} = 2.4 mA, V_{IN+} = 0 V	23	
Input Low Supply Current	I_{CC1L}		3	6	mA	I_F = 0 mA, V_{IN+} = 0 V	1	
Input High Supply Current	I_{CC1H}		3	6	mA	I_F = 10 mA, V_{IN+}=0 V	1	
			13	16	mA	I_{LEDDRV} = 10 mA , V_{IN+}=5 V		
Output Low Supply Current	I_{CC2L}		4.3	6.5	mA	I_F = 0 mA	2, 3	
Output High Supply Current	I_{CC2H}		5.4	7.5	mA	I_F = 10 mA	2, 3	
LED Forward Voltage	V_F	1.2	1.55	1.95	V	I_F =10 mA	4	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.7		mV/°C	I_F = 10 mA		
LED Reverse Breakdown Voltage	V_{BR}	5			V	I_F = 10 μA		
Input Capacitance	C_{IN}		70		pF			
LED Turn on Current Threshold Low to High	I_{TH+}	0.25	2	6	mA	V_{OUT} = 5 V		
LED Turn on Current Threshold High to Low	I_{TH-}	0.15	1.5	5.5	mA	V_{OUT} = 5 V		
LED Turn on Current Hysteresis	I_{TH_HYS}		0.5		mA			
High Level Output Current	I_{OH}	-2	-3.5		A	V_{CC2} - V_{OUT} =15 V		1
Low Level Output Current	I_{OL}	2	3.0		A	V_{OUT} - V_{EE} = 15 V		1
High Output Transistor $R_{DS(ON)}$	$R_{DS,OH}$	0.5	2.5	5.0	Ω	I_{OH} = -2 A		2
Low Output Transistor $R_{DS(ON)}$	$R_{DS,OL}$	0.2	1.8	4.0	Ω	I_{OL} = 2 A		2
Low Level Output Current During Fault Condition	I_{OLF}	55	115	170	mA	V_{OUT} - V_{EE} = 14 V	7	3
High Level Output Voltage	V_{OH}	V_{CC} – 0.5	V_{CC2} – 0.15		V	I_{OUT} = -100 mA	5	4, 5, 6
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_{OUT} = 100 mA	6	
Clamp Threshold Voltage	V_{TH_CLAMP}		2	3	V			
Clamp Low Level Sinking Current	I_{CLAMP}	0.75	1.9		A	V_{CLAMP} = V_{EE} + 2.5		
Clamp Output Transistor $R_{DS(ON)}$	$R_{DS,CLAMP}$		1.1	3.5	Ω	I_{CLAMP} = 1 A		
V_{CC2} UVLO Threshold Low to High	V_{UVLO+}	11	12.5	13.7	V	V_{OUT} > 5 V		4, 6, 7
V_{CC2} UVLO Threshold High to Low	V_{UVLO-}	10.1	11.3	12.8	V	V_{OUT} < 5 V		4, 6, 8
V_{CC2} UVLO Hysteresis	V_{UVLO_HYS}	0.4	1.2		V			
DESAT Detection Threshold	V_{DESAT}	6.2	7	7.8	V		8	6
DESAT Charging Current	I_{CHG}	0.6	1.0	1.2	mA	V_{DESAT} = 2 V	9	6, 9
DESAT Discharging Current	I_{DSCHG}	20	58		mA	V_{DESAT} = 8 V	10	
FAULT Logic Low Output Current	I_{FAULT_L}	4	9.0		mA	V_{FAULT} = 0.4 V		
FAULT Logic High Output Current	I_{FAULT_H}			20	μA	V_{FAULT} = 5 V		
UVLO Logic Low Output Current	I_{UVLO_L}	4	9.0		mA	V_{UVLO} = 0.4 V		
UVLO Logic High Output Current	I_{UVLO_H}			20	μA	V_{UVLO} = 5 V		

Notes:

1. Maximum pulse width = 10 μs.
2. Output is sourced at -2.0 A/2.0 A with a maximum pulse width = 10 μs.
3. For further details, see the description of operation during DESAT fault condition section in the application notes.
4. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} – V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 13.7 V. For High Level Output Voltage testing, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero.
5. Maximum pulse width = 1.0 ms.
6. Once V_{OUT} of ACPL-336J is allowed to go High (V_{CC2} – V_E > V_{UVLO+}), the DESAT detection feature of the ACPL-336J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{CC2} exceeds V_{UVLO+} threshold, DESAT will remain functional until V_{CC2} is below V_{UVLO-} threshold. Thus, the DESAT detection and UVLO features of the ACPL-336J work in conjunction to ensure constant IGBT protection.
7. This is the "increasing" (i.e., turn-on or "positive going" direction) of V_{CC2} – V_E.
8. This is the "decreasing" (i.e., turn-off or "negative going" direction) of V_{CC2} – V_E.
9. For further details, see the DESAT fault detection blanking time section in the applications notes.

Table 6. Switching Specifications (AC)

Unless otherwise noted, all typical values at T_A = 25 °C, V_{CC1} = 5 V, V_{CC2} – V_{EE2} = 30 V, V_E – V_{EE2} = 0 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input LED to High Level Output Propagation Delay Time	t_{PLH}	50	130	220	ns	R_G = 10 Ω, C_G = 10 nF, f = 10 kHz, Duty Cycle = 50%	11, 12, 13	1
Input LED to Low Level Output Propagation Delay Time	t_{PHL}	50	155	250	ns		11, 12, 13	2
Pulse Width Distortion	PWD		25	120	ns			3, 4
Propagation Delay Difference Between Any 2 Parts (t_{PHL}-t_{PLH})	P_{DD}	-150		150	ns			4, 5
Propagation Delay Skew	t_{PSK}			100	ns			4,6
10% to 90% Rise Time	t_R		80		ns			
90% to 10% Fall Time	t_F		45		ns			
DESAT Blanking Time	$t_{DESAT(BLANKING)}$		0.6	1.1	µs		24	7
DESAT Sense to 90% V_{OUT} Delay	$t_{DESAT(90\%)}$		1.3	2	µs	R_G = 10 Ω, C_G= 10 nF	24	8
DESAT Sense to 10% V_{OUT} Delay	$t_{DESAT(10\%)}$		4.8	6.5	µs		24	9
DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT(LOW)}$		0.25		µs		24	10
DESAT Sense to Low Level FAULT Signal Delay	$t_{DESAT(FAULT)}$		2.2	5	µs	R_F = 10 kΩ, C_F = Open	24	11
Output Mute Time due to DESAT	$t_{DESAT(MUTE)}$	2.3	3.0	4.2	ms		24	12
Time Input Kept Low Before Fault Reset to High	$t_{DESAT(RESET)}$	2.3	3.0	4.2	ms	R_F = 10 kΩ, C_F = Open	24	13
V_{CC2} to UVLO High Delay	t_{PLH_UVLO}		10		µs		22	14
V_{CC2} to UVLO Low Delay	t_{PHL_UVLO}		10		µs		22	15
V_{CC2} UVLO to V_{OUT} High Delay	t_{UVLO_ON}		5.3		µs		22	16
V_{CC2} UVLO to V_{OUT} Low Delay	t_{UVLO_OFF}		1		µs		22	17
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	30	>50		kV/µs	T_A = 25 °C, I_F = 10 mA, V_{CM} = 1500 V, V_{CC2} = 30 V	14, 16,18	18, 20
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	30	>50		kV/µs	T_A = 25 °C, I_F = 0 mA, V_{CM} = 1500 V, V_{CC2} = 30 V,	15, 17, 19	19, 20

Notes:

1. t_{PLH} is defined as propagation delay from 50% of LED input I_F to 50% of High level output.
2. t_{PHL} is defined as propagation delay from 50% of LED input I_F to 50% of Low level output.
3. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
4. As measured from I_F to V_{OUT}.
5. The difference between t_{PHL} and t_{PLH} between any two ACPL-336J parts under the same test conditions.
6. t_{PSK} is equal to the worst-case difference in t_{PHL} and t_{PLH} that will be seen between units under the same test condition.
7. The ACPL-336J internal delay time to respond to a DESAT fault condition without any external DESAT capacitor.
8. The amount of time from when DESAT threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.
9. The amount of time from when DESAT threshold is exceeded to 10% of V_{GATE} at mentioned test conditions.
10. The amount of time from when DESAT threshold is exceeded to DESAT Low voltage, 0.7 V.
11. The amount of time from when DESAT threshold is exceeded to FAULT output Low – 50% of V_{CC1} voltage.
12. The amount of time when DESAT threshold is exceeded, output is muted to LED input.
13. The amount of time when DESAT mute time is expired, LED input must be kept low for FAULT status to return to High.
14. The delay time when V_{CC2} exceeds UVLO+ threshold to UVLO high – 50% of UVLO positive-going edge.
15. The delay time when V_{CC2} exceeds UVLO- threshold to UVLO low – 50% of UVLO negative-going edge.
16. The delay time when V_{CC2} exceeds UVLO+ threshold to 50% of high level output.
17. The delay time when V_{CC2} exceeds UVLO- threshold to 50% of low level output.
18. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_{OUT} > 15 V or FAULT > 2 V or UVLO > 2 V). A 330 pF and a 10 kΩ pull-up resistor are needed in FAULT and UVLO detection mode.
19. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_{OUT} < 1.0 V or FAULT < 0.8 V or UVLO < 0.8 V).
20. Split resistor network in the ratio 1:1 at the anode and cathode. For further details, see description of input LED driver and split resistors circuit section in the application notes.

Table 7. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min., T_A = 25 °C	1, 2, 3
Resistance (Input-Output)	R_{I-O}		> 10^9		Ω	V_{I-O} = 500 V_{DC}	3
Capacitance (Input-Output)	C_{I-O}		1.3		pF	freq =1 MHz	
Thermal Coefficient Between							4
LED and Input IC	A_{EI}		35.4		°C/W		
LED and Output IC	A_{EO}		33.1		°C/W		
Input IC and Output IC	A_{IO}		25.6		°C/W		
LED and Ambient	A_{EA}		176.1		°C/W		
Input IC and Ambient	A_{IA}		92		°C/W		
Output IC and Ambient	A_{OA}		76.7		°C/W		

Notes

1. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table, if applicable.
2. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.
3. Device considered a two-terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
4. For further details, see thermal calculation section in the application notes.

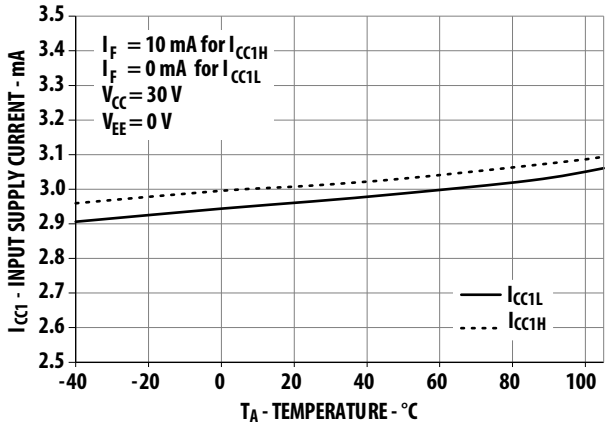


Figure 1. I_{CC1} vs. temperature

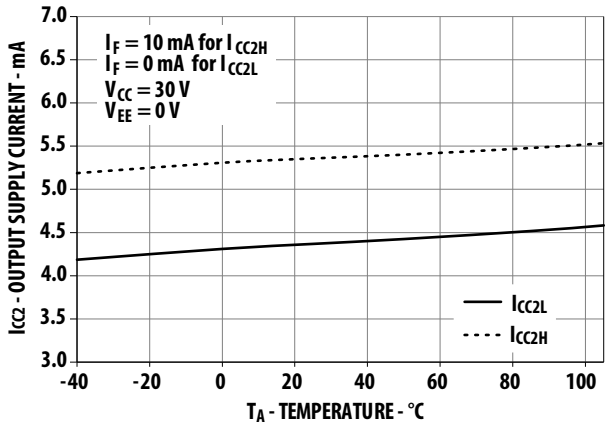


Figure 2. I_{CC2} vs. temperature

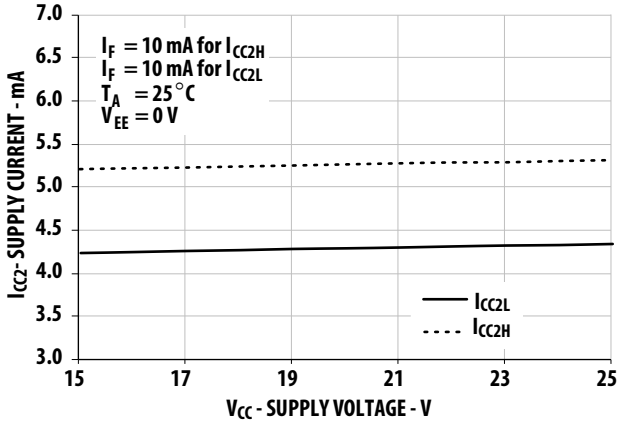


Figure 3. I_{CC} vs. V_{CC}

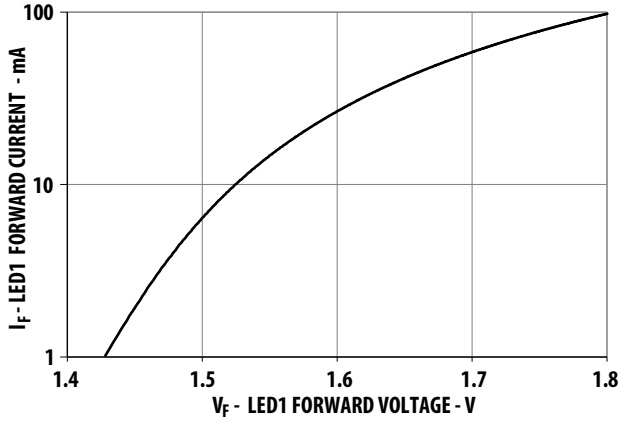


Figure 4. LED1 Input Current vs. forward voltage

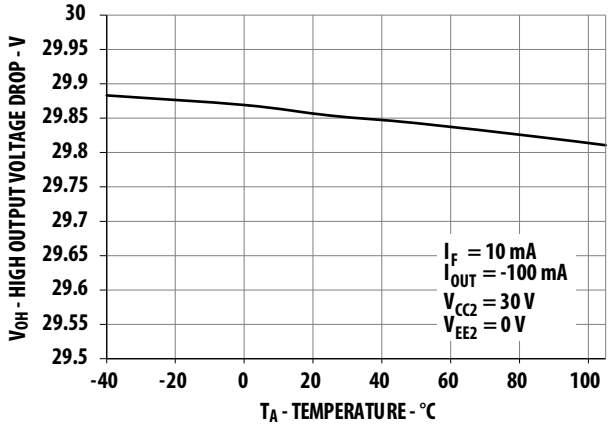


Figure 5. V_{OH} vs. temperature

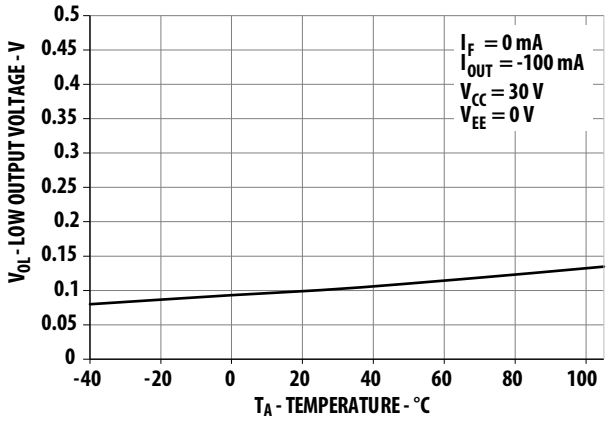


Figure 6. V_{OL} vs. temperature

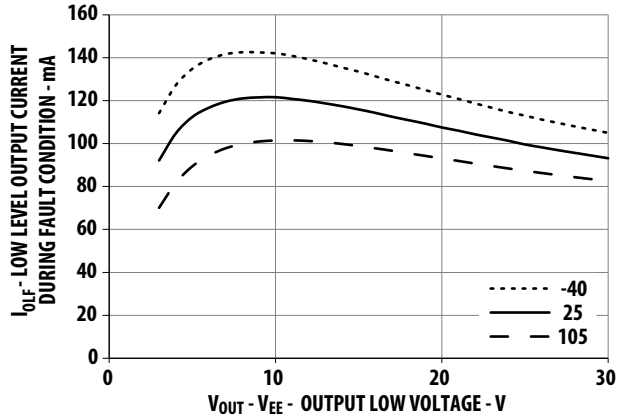


Figure 7. I_{OLF} vs. output voltage

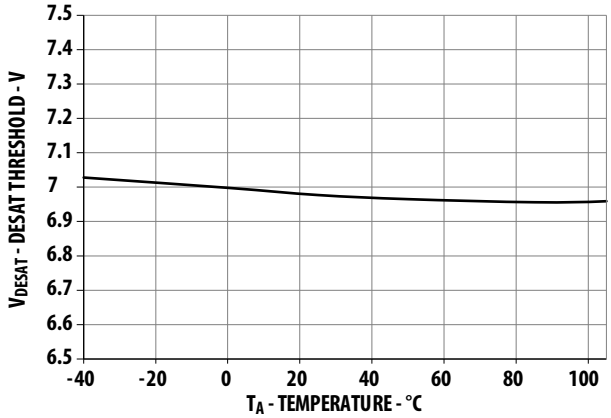


Figure 8. V_{DESAT} vs. temperature

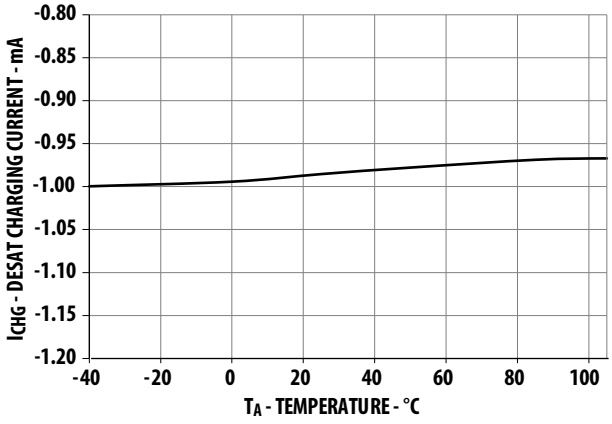


Figure 9. I_{CHG} vs. temperature

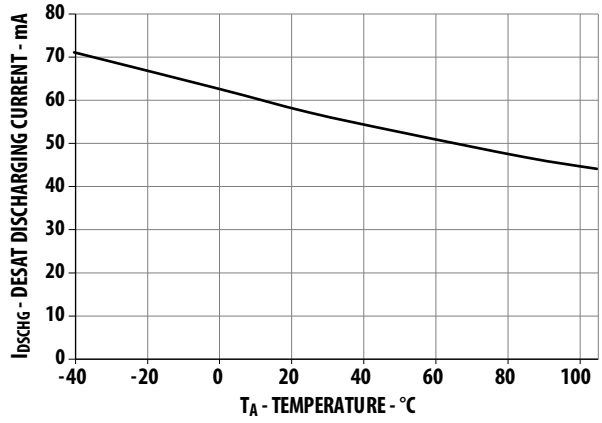


Figure 10. I_{DSCHG} vs. temperature

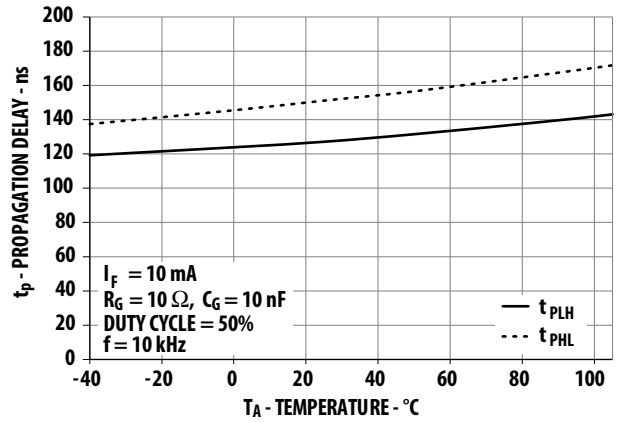


Figure 11. Propagation delay vs. temperature

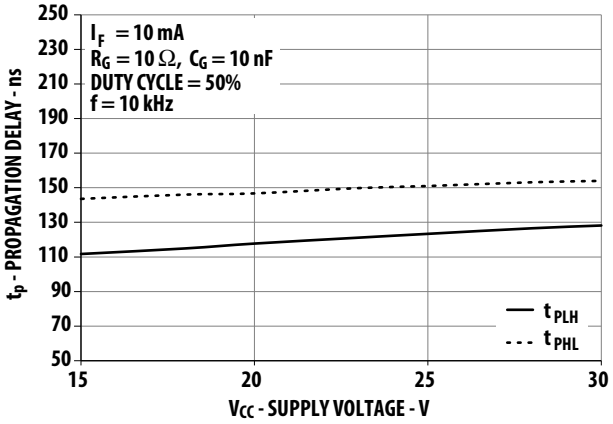


Figure 12. Propagation delay vs. supply voltage

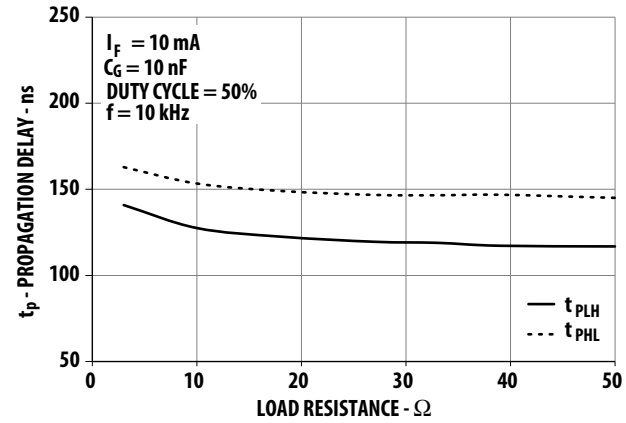


Figure 13. Propagation delay vs. load resistance

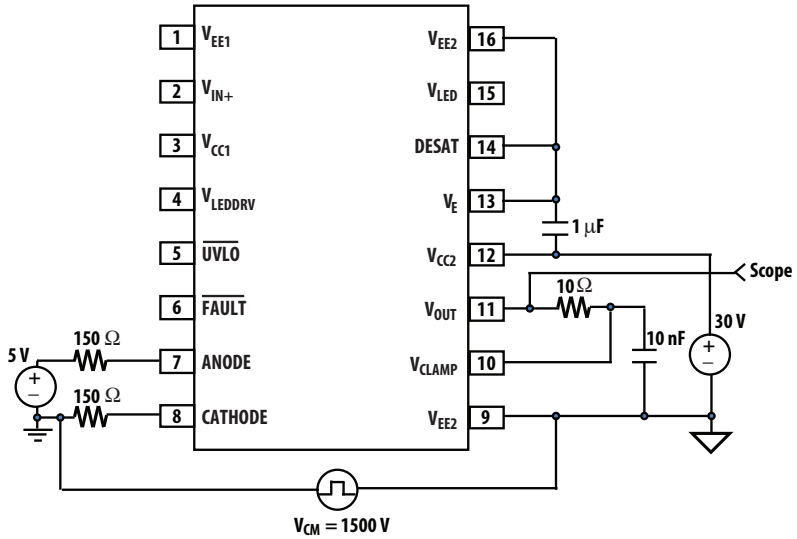


Figure 14. CMR V_{OUT} High test circuit

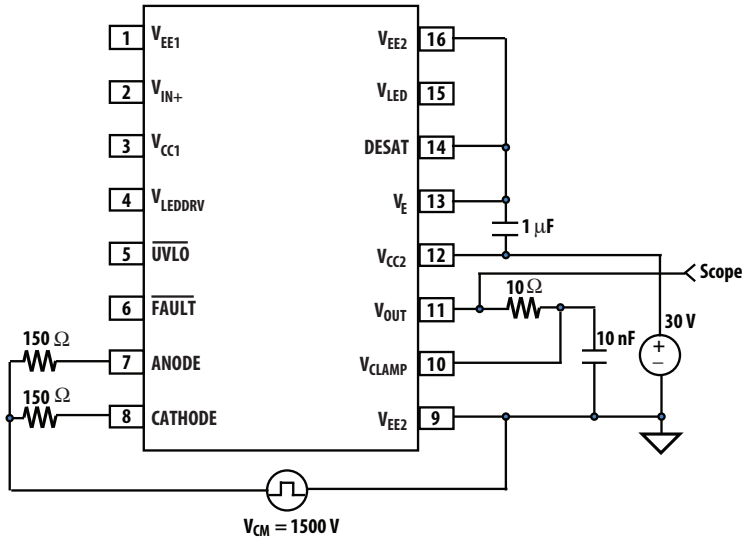


Figure 15. CMR V_{OUT} Low test circuit

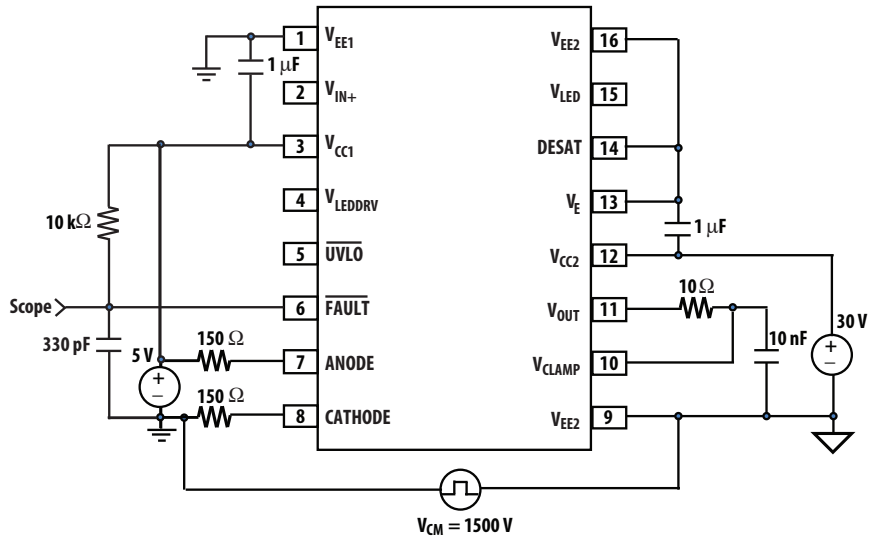


Figure 16. CMR FAULT High test circuit

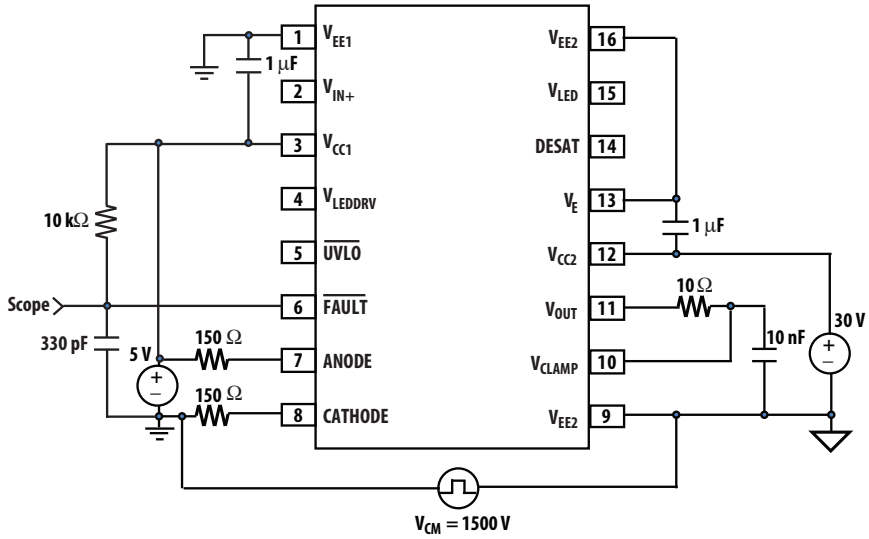


Figure 17. CMR FAULT Low test circuit

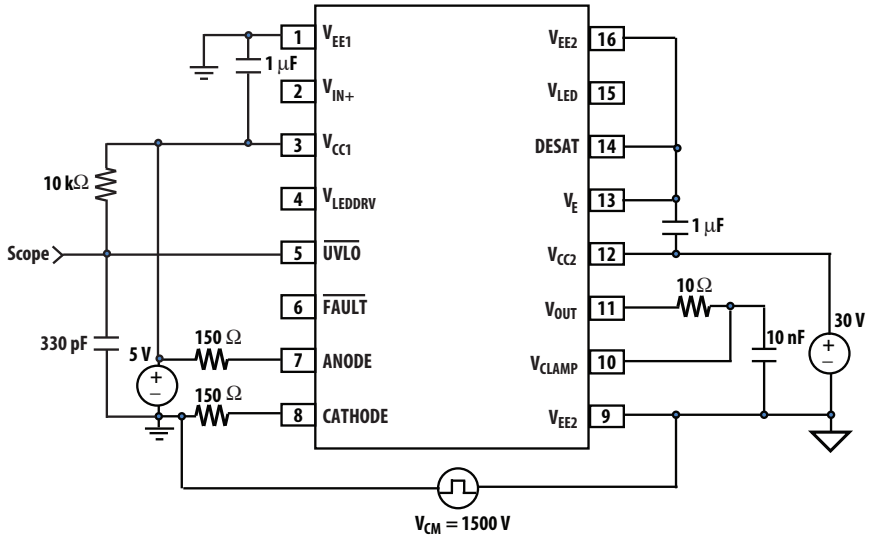


Figure 18. CMR UVLO High test circuit

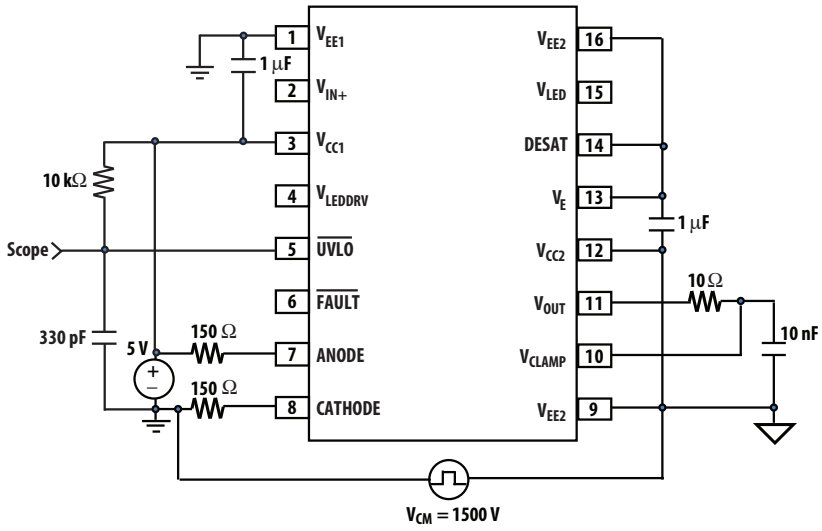


Figure 19. CMR UVLO Low test circuit

Applications Information

Recommended Application Circuit

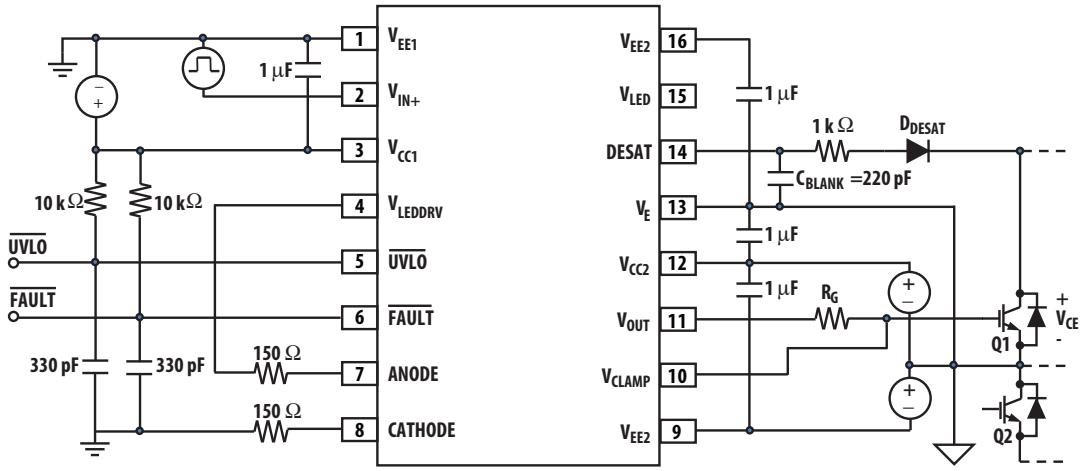


Figure 20. Typical gate drive circuits with DESAT detection

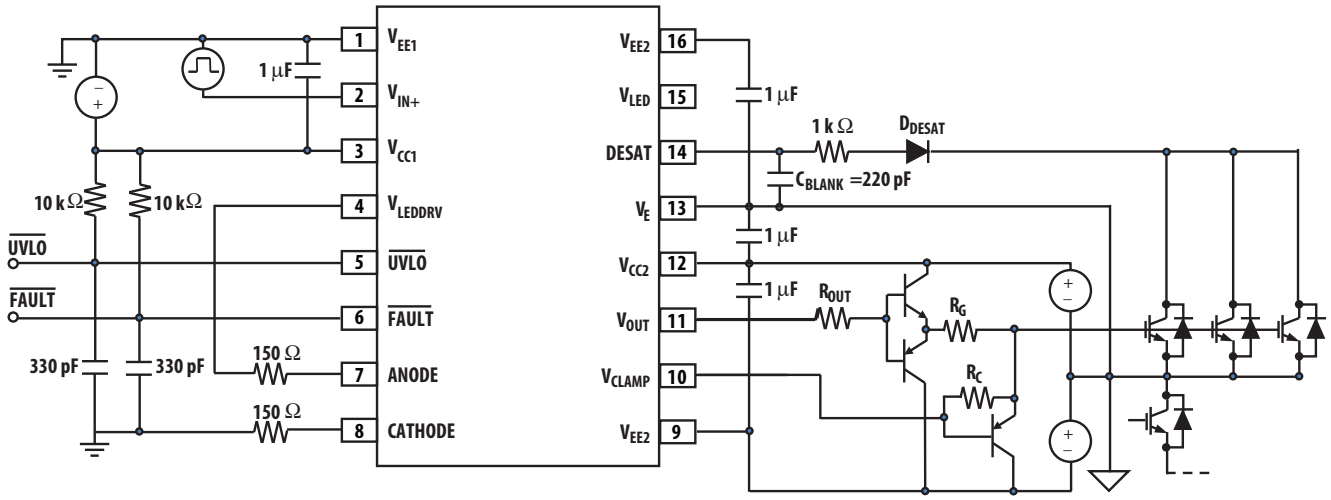


Figure 21. Typical parallel IGBT gate drive circuits with DESAT detection

The ACPL-336J has non-inverting gate control inputs, and an open drain FAULT and UVLO outputs suitable for wired 'OR' applications. The two supplies bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. The DESAT diode and 220 pF blanking capacitor are the necessary external components for the fault detection circuitry. The gate resistor (R_G) serves to limit gate charge current and indirectly control the IGBT collector voltage rise and fall times. The open drain FAULT and UVLO outputs have passive 10kΩ pull-up resistors and a 330 pF filtering capacitor.

Introduction to DESAT Detection

The power stage of a typical three phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector to emitter voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the IGBTs during a fault condition.

A circuit providing fast local DESAT detection and shutdown is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features that this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size. The ACPL-336J satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shut down, and optically isolated fault and UVLO status feedback signal into a single 16-pin surface mount package.

The fault detection method, which is adopted in the ACPL-336J, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false 'fault' signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ACPL-336J limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly-conservative overcurrent threshold is not needed to protect the IGBT.

Output Control

The outputs (V_{OUT}, $\overline{FAULT}$ and $\overline{UVLO}$) of the ACPL-336J are controlled by the combination of V_{CC1}, V_{CC2}(UVLO), LED current I_F and IGBT desaturation condition. The following table shows the logic truth table for these outputs.

V_{CC1}	V_{CC2} (UVLO)	I_F	DESAT	V_{OUT}	$\overline{Fault}$	$\overline{UVLO}$
Low	Low	X	Not Active	Low	Low	Low
Low	High	Low	Not Active	Low	Low	Low
Low	High	High	Active (no DESAT fault)	High	Low	Low
Low	High	High	Active (DESAT fault)	Low	Low	Low
High	Low	X	Not Actve	Low	High	Low
High	High	High	Active (DESAT fault)	Low	Low	High
High	High	Low	Not Active	Low	High	High
High	High	High	Active (no DESAT fault)	High	High	High

The logic level is defined by the respective threshold of each function pin.

Description of UnderVoltage LockOut

Insufficient gate voltage to IGBT can increase turn-on resistance of IGBT, resulting in large power loss and IGBT damage due to high heat dissipation. ACPL-336J monitors the output power supply constantly. When output power supply is lower than undervoltage lockout (UVLO) threshold, the gate driver output will shut off to protect IGBT from low voltage bias. The low output power supply fault will be reported via the UVLO feedback. In this way, the UVLO feedback can also serve as a READY signal to the controller during power up.

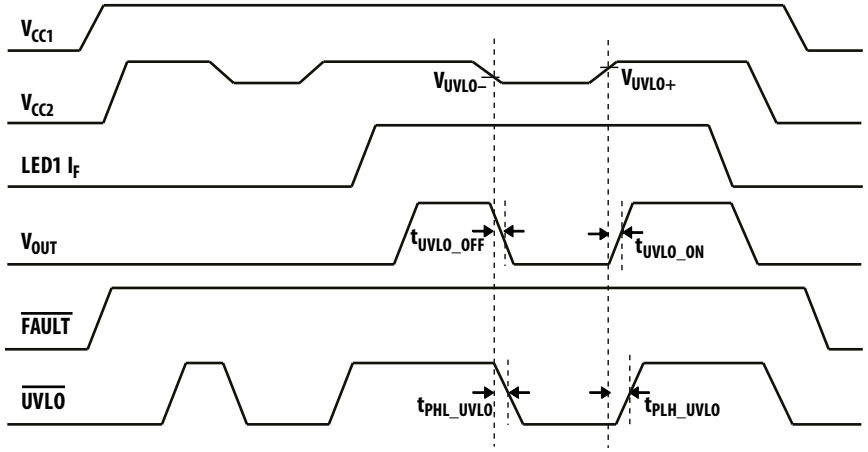
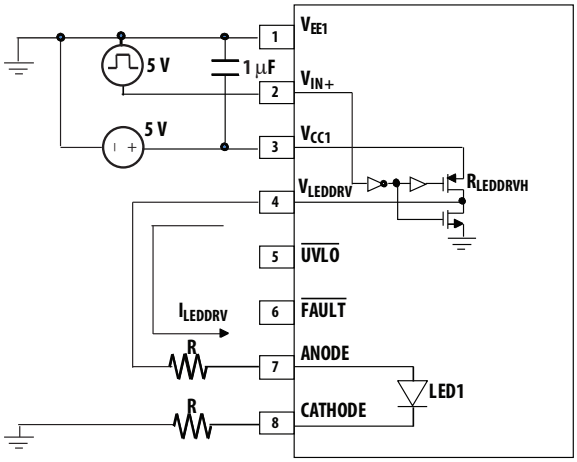


Figure 22. UVLO and feedback behaviors and timing diagram

Description of Input LED Driver and Split Resistors Circuit

The ACPL-336J has integrated an input LED driver that with high impedance input(V_{IN+}) for interfacing with the controller. The LED driver's output(V_{LEDDRV}) has to be connected with the recommended split resistors circuit to the LED1 anode to achieve the rated high CMR performance. The LED current can be calculated by $I_{LEDDRV} = (V_{CC1} - V_F)/(R_{LEDDRVH} + 2R)$. Alternatively, if the LED driver is not used, LED1 can still be driven directly by other means of discrete driver configuration.

It is recommended that the two resistors (R) connected to input LED's anode and cathode are split in the ratio 1:1. They will help to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage changes at the anode and cathode to give high CMR performance.



$$I_{LEDDRV} = (V_{CC1} - V_F)/(R_{LEDDRVH} + 2R)$$

Figure 23. Input LED driver functional diagram

DESAT Fault Detection Blanking Time

The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT theshold. This time period, called the DESAT blanking time, is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor.

The nominal blanking time is calculated in terms of external capacitance (C_{BLANK}, see Figure 20 and Figure 21), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) in addition to an internal DESAT blanking time ($t_{DESAT(BLANKING)}$).

$t_{BLANK} = C_{BLANK} \times (V_{DESAT}/I_{CHG}) + t_{DESAT(BLANKING)}$

Description of Operation during DESAT Fault Condition

1. DESAT terminal monitors IGBT's V_{CE} voltage.
2. When the voltage on the DESAT terminal exceeds 7 V, a weak pull-down in the output stage(I_{OLF}) will turn on to 'softly' turn off the IGBT. When the gate voltage falls below V_{EE}+2 V, the Miller Clamp will turn on to clamp the IGBT gate to V_{EE}.
3. FAULT output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.
5. When $t_{DESAT(MUTE)}$ expires, LED input needs to be kept low for $t_{DESAT(RESET)}$ before fault condition is cleared. FAULT status will return to high.
6. Output (V_{OUT}) starts to respond to LED input after fault condition is cleared.

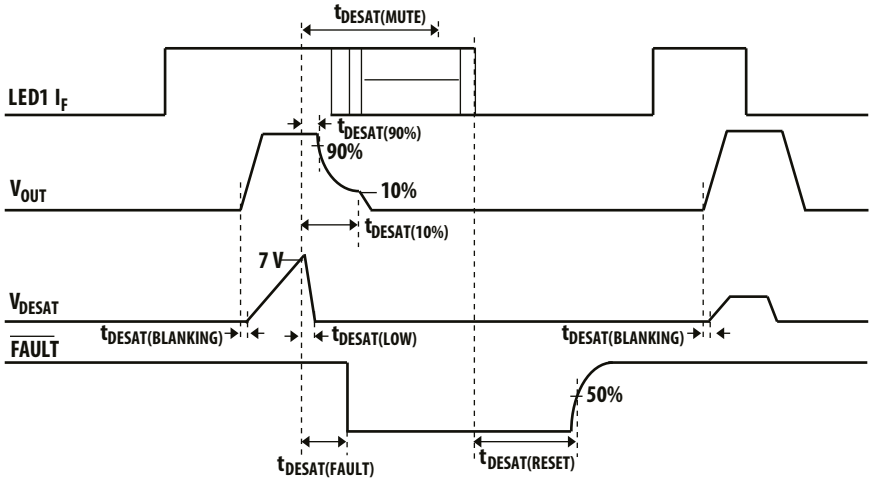


Figure 24. DESAT fault state timing diagram

Selecting the Gate Resistor (R_G)

Step 1: Calculate R_G minimum from the $I_{O(PEAK)}$ specification. The IGBT and R_G in Figure 20 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-336J.

$$R_G \geq \frac{V_{CC} - V_{EE}}{I_{O(PEAK)}} - R_{DS,OH(MIN)}$$

$$= \frac{30\ V - 0\ V}{2.5\ A} - 0.5\ \Omega$$

$$= 11.5\ \Omega$$

or

$$R_G \geq \frac{V_{CC} - V_{EE}}{I_{O(PEAK)}} - R_{DS,OL(MIN)}$$

$$= \frac{30\ V - 0\ V}{2.5\ A} - 0.2\ \Omega$$

$$= 11.8\ \Omega$$

The external gate resistor, R_G and internal minimum turn-on resistance, R_{DSON} will ensure the output current will not exceed the device absolute maximum rating of 2.5 A. In this case, we will use worst-case $R_G \geq 11.8\ \Omega$.

Step 2: Check the ACPL-336J power dissipation and increase R_G if necessary. The ACPL-336J total power dissipation (P_T) is equal to the sum of the LED power (P_E), input IC power(P_I) and the output IC power (P_O).

$P_T = P_E + P_I + P_O$

Assuming operation conditions of I_F(worst case) = 16 mA, R_G = 11.8 Ω, Max Duty Cycle = 80%, Q_G = 1 μC, f = 10 kHz and T_A max = 95 °C.

Calculation of LED Power Dissipation

$P_E = I_F \cdot V_F \cdot$ Duty Cycle

$= 16 \text{ mA} \cdot 1.95 \text{ V} \cdot 0.8 = 25 \text{ mW}$

Calculation of Input IC Power Dissipation

$P_I = I_{CC1}$(Max) * V_{CC1}(Recommended Max)

$= 6 \text{ mA} * 5.5 \text{ V} = 33 \text{ mW}$

Calculation of Input IC Power Dissipation

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$

$= I_{CC2} \cdot (V_{CC2}-V_{EE2}) + P_{HS} + P_{LS}$

$P_{HS} = (V_{CC2}*Q_G*f) * R_{DS,OH(MAX)} / (R_{DS,OH(MAX)}+R_G) / 2$

$P_{LS} = (V_{CC2}*Q_G*f) * R_{DS,OL(MAX)} / (R_{DS,OL(MAX)}+R_G) / 2$

$P_{HS} = (30 \text{ V} \cdot 1\mu\text{C} \cdot 10 \text{ kHz}) \cdot 4.5 \Omega/(4.5 \Omega + 7.3 \Omega)/2 = 44.6 \text{ mW}$

$P_{LS} = (30 \text{ V} \cdot 1\mu\text{C} \cdot 10 \text{ kHz}) \cdot 3.6 \Omega/(3.6 \Omega + 7.3 \Omega)/2 = 38.0 \text{ mW}$

$P_O = 7.5 \text{ mA} \cdot 30 \text{ V} + 44.6 \text{ mW} + 38.0 \text{ mW}$

$= 307.6 \text{ mW} < 600 \text{ mW}$ ($P_{O(MAX)}$ @ 95 °C)

The value of 7.5 mA for I_{CC2} in the previous equation is the maximum I_{CC2} over the entire operating temperature range.

Since P_O is less than $P_{O(MAX)}$, R_G = 11.8 Ω is all right for the power dissipation.

Thermal Calculation

Application and environmental design for ACPL-336J needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 125 °C. The following equations calculate the maximum power dissipation effect on junction temperatures.

LED Junction Temperature, $T_E = A_{EA}*P_E + A_{EI}*P_I + A_{EO}*P_O + T_A$

$= 176.1 \text{ °C/W} * 25 \text{ mW} + 35.4 \text{ °C/W} * 33 \text{ mW} + 33.1 \text{ °C/W} * 307.6 \text{ mW} + 95 \text{ °C}$

$= 110.7 \text{ °C}$

Input IC Junction Temperature, $T_I = A_{EI}*P_E + A_{IA}*P_I + A_{IO}*P_O + T_A$

$= 35.4 \text{ °C/W} * 25 \text{ mW} + 92 \text{ °C/W} * 33 \text{ mW} + 25.6 * 307.6 \text{ mW} + 95 \text{ °C}$

$= 106.8 \text{ °C}$

Output IC Junction Temperature, $T_O = A_{EO}*P_E + A_{IO}*P_I + A_{OA}*P_O + T_A$

$= 33.1 \text{ °C/W} * 25 \text{ mW} + 25.6 \text{ °C/W} * 33 \text{ mW} + 76.7 * 307.6 \text{ mW} + 95 \text{ °C}$

$= 120.3 \text{ °C}$

DESAT Diode and DESAT Threshold

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage, V_{CESAT}, (when the IGBT is "on") and to block high voltages (when the IGBT is "off").

When the IGBT is switching off and toward the end of the forward conduction of the DESAT diode, a reverse current will flow for short time. This reverse recovery effect prevents the diode from achieving its blocking capability until the mobile charge in the junction is depleted. During this time, there is commonly a very high dV_{CE}/dt voltage ramp rate across the IGBT's collector-to-emitter. This results in $I_{CHARGE} = C_{D\text{-}DESAT} \times dV_{CE}/dt$ charging current which will charge the blanking capacitor, C_{BLANK}. To minimize this charging current and avoid false DESAT triggering, it is best to use fast-response diodes.

In the recommended application circuit shown in Figure 20, the voltage on pin 14 (DESAT) is $V_{DESAT} = V_F + V_{CE}$, where V_F is the forward ON voltage of D_{DESAT} and V_{CE} is the IGBT collector-to-emitter voltage. The value of V_{CE} that triggers DESAT to signal a FAULT condition is nominally 7 V – V_F. If desired, this DESAT threshold voltage can be decreased by using multiple DESAT diodes or low-voltage Zener diode in series. If n is the number of DESAT diodes, the nominal threshold value becomes $V_{CE,FAULT(TH)} = 7\ V - n \times V_F$. If a Zener diode is used, the nominal threshold value becomes $V_{CE,FAULT(TH)} = 7\ V - V_F - V_Z$. When using two diodes instead of one, then diodes with half of the total required maximum reverse-voltage rating may be chosen.

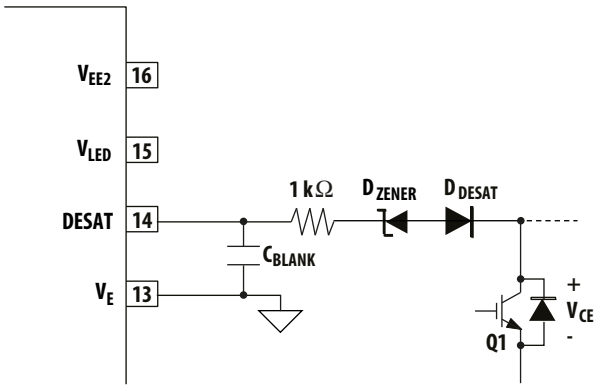


Figure 25. DESAT diode and DESAT threshold

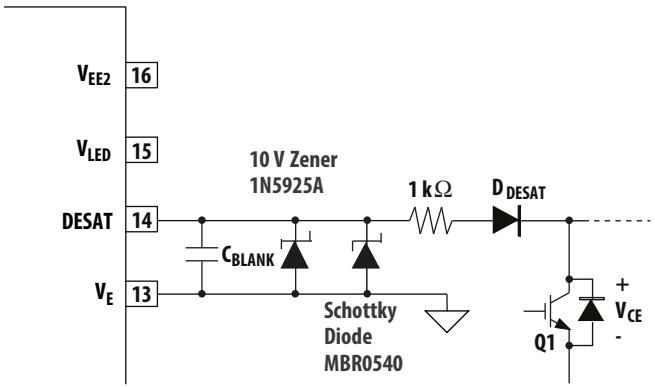


Figure 26. False fault prevention diodes

DESAT Pin Protection Resistor

The freewheeling of flyback diodes connected across the IGBTs can have large instantaneous forward voltage transients that greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin, which will draw substantial current out of the driver if protection is not used. To limit this current to levels that will not damage the driver IC, make sure a 1 kΩ resistor is inserted in series with the DESAT diode.

False Fault Prevention Diodes

A situation that may cause the driver to generate a false fault signal is if the substrate diode of the driver becomes forward biased. This can happen if the reverse recovery spikes coming from the IGBT freewheeling diodes bring the DESAT pin below Ground. Therefore, the DESAT pin voltage will be 'brought' above the threshold voltage. This negative going voltage spikes are typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFETs free-wheeling diodes. To prevent a false fault signal, it is highly recommended that you connect a Zener diode and a Schottky diode across the DESAT pin and V_E pin

Figure 26 shows this circuit solution. The Schottky diode will prevent the substrate diode of the gate driver optocoupler from being forward biased while the Zener diode (10 V) is used to prevent any positive high transient voltage from affecting the DESAT pin.

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